

**IN THE CLAIMS**

**Please cancel claims 1-7. The claims are as follows:**

**1-7 (CANCELED)**

**8. (Original) An active restore circuit for write margin testing of an SRAM having a bitline restore driver comprising:**

**a NAND gate connected to the bitline restore driver having three terminals;**

**a write margin test signal is applied to the first NAND gate terminal to activate the margin test;**

**a sub array clock signal (COLSEC) is applied to the second terminal of the NAND gate which generates a restore signal to the bitline restore driver to block the bitline restore devices from turning off during the SRAM write cycle.**

**9. (Original) The circuit of claim 8 which includes two transistors in the bitline restore driver to assist the bitline driver to block the bitline restore devices from turning off.**

**10. (Original) The circuit of claim 9 wherein cells are identified if they fail the write test margin test.**

**11. (Original) The circuit of claim 10 wherein the identified failed cells are replaced with redundant memory elements.**